What is claimed is:

1. A semiconductor memory device operating in synchronization with an external clock signal, comprising:

memory cells arrayed in two dimension;

word lines and bit lines connected to the memory cells;

IO lines connected to the bit lines; and

a sense amplifier connected to the IO lines and activated by a sense amplifier enable signal,

wherein after the word line is selected, an internal clock signal is generated by delaying the rising and falling edges of the external clock signal input to the memory device, and

wherein a timing at which the internal clock signal changes from a first state to a second state is delayed by a predetermined time to make the sense amplifier enable signal active, and a timing at which the internal clock signal changes from the second state to the first state is delayed by a shorter period than the predetermined time to make the sense amplifier enable signal inactive.

2. The semiconductor memory device according to claim 1, wherein potential of the IO lines are initialized before the word line is selected, the initialization of the

IO lines are terminated according to the selection of the word line, and the IO lines are initialized again according to the change of the external clock signal from the second state to the first state and the inactivation of the sense amplifier enable signal.

3. A semiconductor memory device operating in synchronization with an external clock signal, comprising:

memory cells arrayed in two dimension;

word lines and bit lines connected to memory cells;

IO lines connected to bit lines;

a sense amplifier connected to the IO lines and activated by a sense amplifier enable signal;

a first delay circuit operable to delay an internal clock signal by a first predetermined time, the internal clock signal being generated by delaying the rising and falling edges of the external clock signal input to the memory device after the word line is selected;

a second delay circuit operable to delay the internal clock signal by a second predetermined time; and

an AND circuit operable to logically multiply an output signal from the first delay circuit and an output signal from the second delay circuit to generate the sense amplifier enable signal.

4. The semiconductor memory device according to claim 3, wherein the first or second delay circuit comprises a delay stages including multiple stages of delay elements and the number of delay stages can be modified by changing the wiring pattern of the delay stages.